

# The Use of Boron Nitride for Field Effect Electron Emission

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**Boron nitride in the cubic phase has been considered a potential candidate for use as electron field emitters. This paper highlights results and challenges in characterizing boron nitride's suitability for use in electric propulsion applications and in designing and fabricating the gated electrodes needed to extract and accelerate the electrons.**

## Nomenclature

$A$	= aspect ratio	$I$	= emission current
$A_e$	= emission area	$J$	= current density
$A_{FN}, B_{FN}$	= Fowler-Nordheim coefficients	$m_{FN}$	= Fowler-Nordheim slope
$d$	= gap distance	$R$	= emission channel radius
$D$	= emission channel diameter	$\beta$	= field enhancement factor
$E_s$	= emission surface electric field	$\phi_w$	= work function
$H$	= emission channel height		

## I. Introduction

A variety of space applications can benefit from cold cathode electron emission, particularly applications such as miniature electric propulsion, where the power or propellant cost of state-of-the-art electron emitters (e.g., thermionic or hollow cathodes) are too high for a viable system design. Cold cathode emitters extract electrons by the application of high electric fields at a conducting surface. They utilize microfabrication techniques to achieve gate proximity and emission tip geometry that allow the necessary field strength to be created at modest voltages. Requiring no heaters or ionizable gas sources, cold cathode neutralizers can significantly improve the efficiency of low-power Hall thrusters.<sup>1</sup>

The current state-of-the-art for cold cathode electron emission is the field emitter array, which is composed of millions of silicon or molybdenum nanotips per square centimeter on a semiconductor substrate with an integrated

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gate structure. These devices provide very efficient electron emission but are fragile. The tips have poor sputter resistance and reactive surfaces that limit their lifetime. Consequently, the use of them in a miniature electric propulsion system's plasma environment is troublesome, since ion bombardment of the array would quickly degrade the array tips.<sup>2</sup> Recently, boron nitride in the cubic phase has emerged as a candidate material that could make practical field emission cathodes realizable.<sup>3</sup>

## II. Cubic Boron Nitride

The last decade has seen a marked increase in the research effort towards engineering of the III-V compound semiconductors. Many of these materials exhibit interesting synergies between semiconducting behavior and thermal, mechanical, chemical, and other properties. Cubic boron nitride (c-BN) is one such member of the III-V compound semiconductor family.

Under equilibrium conditions, boron nitride (BN) stabilizes in a hexagonal phase as a soft, insulating material with a crystallographic structure similar to that of graphite.<sup>4</sup> However, when BN is nucleated in the cubic phase, the resulting metastable material is a semiconductor with a wide, indirect band gap of 6.3 eV. With physical properties resembling diamond, c-BN is a candidate material for field emission cathodes (FECs) in electric propulsion (EP) and Low Earth Orbit (LEO) environments.

In these environments, the survivability of FECs in the presence of ion bombardment or contamination is an important concern. The sputtering threshold of c-BN, estimated to be greater than 150 eV, is larger than that of common refractory metals and field emission materials. In addition to having improved sputtering resistance, the chemical inertness of c-BN would make it more tolerant than other prospective emitter materials to atomic oxygen and other contaminants in the operating environment.

Cubic BN has other advantages as a FEC material. Its mechanical toughness would lower ion bombardment damage and inhibit the formation and migration of emitter surface nanoprotusions that could otherwise lead to destructive arcing of the array. A low estimated work function (~2 eV) would enable lower operating voltages to further decrease potential sputtering damage.

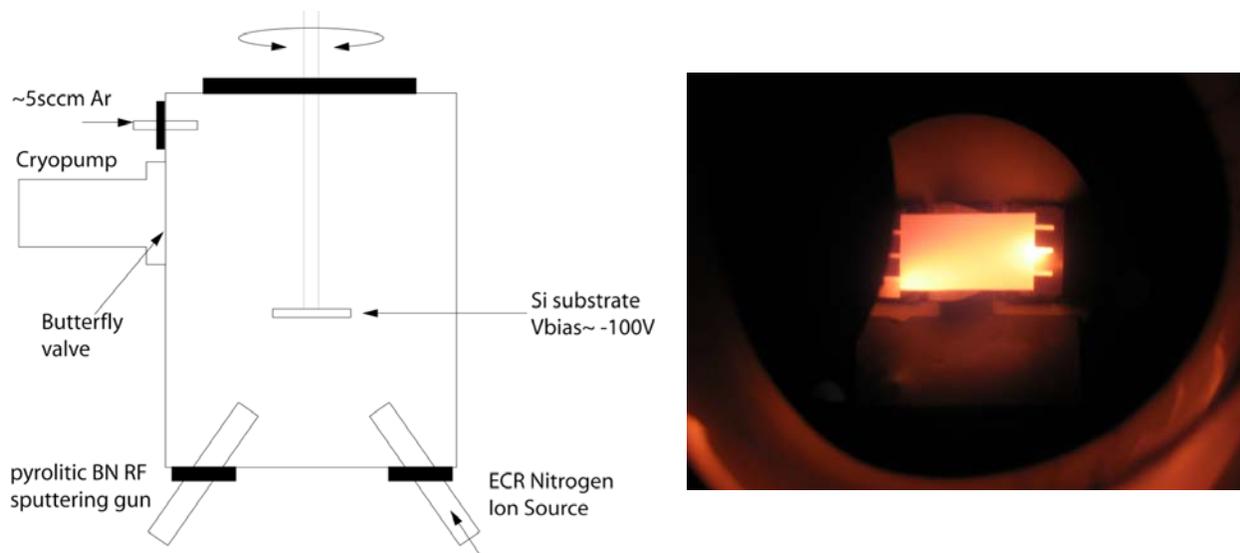
Unfortunately, c-BN is a difficult material to synthesize. A number of methods to grow c-BN thin films have been developed in the past decades with limited success. The major challenge is inducing the nucleation of the cubic phase while optimizing the stress buildup in the film.

### A. Film Growth Process

Cubic BN films were grown using ion-assisted sputtering.<sup>5</sup> Silicon (001) substrates doped to a resistivity of 1-20  $\Omega$ -cm were heated to 1,100 °C prior to film growth to desorb the native oxide layer. After thermal desorption, the temperature was gradually ramped down to ~975 °C for film deposition. Direct heating of the substrate was achieved by passing current (~12 A) through the substrate. To improve film uniformity despite the inherent bias gradient (~9 V) due to the current flow, the backsides of the silicon substrates were coated with platinum on a titanium layer. This coating facilitated driving the silicon into the intrinsic generation regime during the initial temperature ramp up and also provided good electrical contact when testing the c-BN films' electrical characteristics.

Hot pressed pyrolytic BN of 4N purity in the hexagonal phase (h-BN) was used as the sputtering target in a radio-frequency magnetron sputtering gun. The deposition process was performed in a low pressure (~2.5 mTorr) argon (8-sccm flow) and nitrogen (6-sccm flow) environment. To maintain the proper stoichiometry and promote the nucleation of the cubic phase, an electron cyclotron resonance nitrogen ion source was used. The kinetic energy of the incident nitrogen ions was controlled using a voltage bias (~140 VDC) applied to the substrate. Since both cubic and hexagonal phases nucleate simultaneously, the bias favored the selective etching of the softer h-BN while leaving the c-BN material intact.

A growth rate of ~20 nm/hr was achieved. Throughout the deposition process, the substrate temperature was monitored with an optical pyrometer. Because of the high strain in the film, the samples were gradually cooled at less than 10 °C/min to minimize delamination. Afterwards, Fourier transform infrared spectroscopy and energy dispersive spectroscopy were used to evaluate the film composition. Figure 1 shows the deposition chamber setup.



**Figure 1. Growing c-BN films.** (Left) Schematic of deposition chamber setup. (Right) View of heated c-BN sample during deposition.

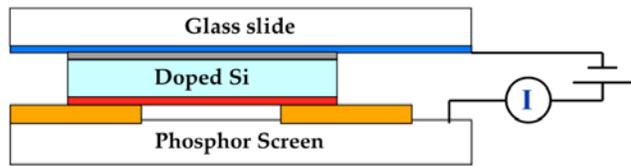
While the flux of nitrogen ions was relatively directional in the deposition chamber, the flux of sputtered BN target material varied due to the asymmetric position of the sputtering source relative to the deposition substrate. Grown samples have been observed with a factor of two difference in film thickness across the sample. As shown in Figure 2, film uniformity was greatly increased by rotating ( $\sim 1$  rev/hr) the substrate during the deposition process.



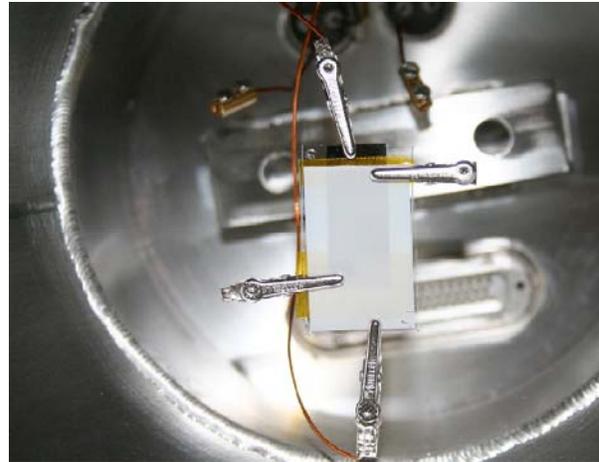
**Figure 2. Effect of substrate rotation during film growth.** (Left) Poor film uniformity without rotation. (Right) Good film uniformity with rotation.

### B. Electron Emission Testing

Field emission characteristics of grown BN films were determined via emission testing in an ultra-high vacuum (UHV) chamber with an operating pressure less than  $10^{-8}$  torr. Figure 3 shows the emission test setup. The BN film on its silicon substrate was offset, using 25- $\mu\text{m}$  spacer made of kapton or Duralar film, from the phosphor screen used to visualize electron emission. The spacer covered up nonuniform regions of the BN film at the edges of the silicon substrate and exposed the remainder of the film ( $\sim 1\text{-}2$   $\text{cm}^2$ ) as available emission area. Vent paths were provided to permit escape of outgassed material from the BN surface during vacuum operations. A glass slide with indium tin oxide (ITO) coating provided electrical contact to the emission sample through the platinum coating. Clamps between the ITO slide and the phosphor screen anode provided planar alignment.

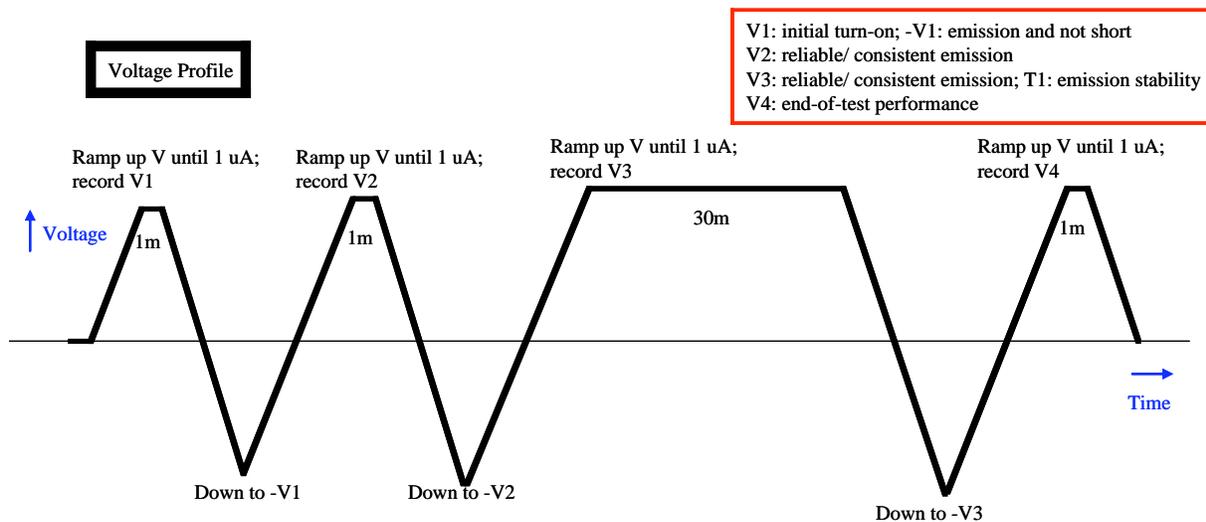


- Pt contact pad
- BN film
- Kapton film spacer (25- $\mu\text{m}$ )
- ITO film



**Figure 3. Field emission characterization setup in UHV chamber.** (Left) Schematic (not to scale) of test setup. (Right) Top view of test setup.

During electron emission characterization, the voltage bias between the BN film and the collection anode was increased until  $\sim 1 \mu\text{A}$  of emission current was obtained from the Keithley 2410 sourcemeter. A series of voltage sweeps, as shown in Figure 4, was conducted to evaluate emission consistency and stability. Negative voltage sweeps were conducted to confirm that measured currents were due to field emission rather than electrical shorts in the system.



**Figure 4. Voltage bias profile for BN films during emission characterization.** Units of time during plateau regions are in minutes (m).

Figure 5 shows a typical scanning electron microscopy (SEM) image of the BN film. Previous test results suggested that thin BN films less than 100 nm in film thickness are promising candidates for electron emission due to their greater surface roughness.<sup>6</sup> For these thin films, the BN composition is a mixture, with c-BN nucleation on a wetting layer of amorphous and hexagonal BN. These “islands” of c-BN nucleation sites have not yet coalesced, and their sharp edges are promising candidates for field emission sites. Although these favorable sites are prevalent throughout the film, Figure 5 shows that only a few isolated sites are activated during emission testing, possibly due to non-uniformities (e.g., concentration of h-BN) not visible in the SEM scans. Non-uniformities in the applied electric field due to compression of the dielectric spacers and surface roughness on the phosphor screen have been evaluated and are not considered significant contributors to the results. Diagnostics to map the chemical and phase compositions of the BN film are being pursued to understand this phenomenon.



**Figure 5. Typical emission characterization results.** (Left) SEM image of BN film. (Right) Emission spots imaged on phosphor screen.

### C. Plasma Environment Survivability

The survivability of c-BN in an EP thruster’s operating environment was tested during thrust characterization of the H6 laboratory model Hall thruster, a 6-kW system jointly developed by the Air Force Research Laboratory, NASA Jet Propulsion Laboratory, and the University of Michigan’s Plasmadynamics and Electric Propulsion Laboratory (PEPL).<sup>7</sup> Testing was conducted in the Large Vacuum Test Facility (LVTF) at PEPL. Vacuum levels of the order  $10^{-5}$  Torr were achieved during the thruster firings.

BN samples were first characterized for field emission properties in the UHV chamber before being partially masked with a tantalum sleeve. Therefore, only part of each BN sample was exposed to the Hall thruster environment, thus facilitating characterization of morphology changes due to plasma exposure. The BN samples were then placed near the H6 thruster, electrically grounded to the chamber walls, and passively exposed during thruster firings. Langmuir probes in the vicinity of the BN samples provided localized plasma diagnostics. Following completion of thruster firings, the BN samples were removed from the LVTF and their field emission properties were reevaluated in the UHV chamber. Of the nine BN samples tested in this manner, five of the samples exhibited better field emission performance following plasma exposure than before. This behavior was surprising, since the expectation was that emission performance would degrade due to the three days of exposure to the LVTF test environment (i.e., plasma and sputtered contaminants from the thruster, outgassing, etc.).

As a case study, Figure 6 shows one such BN sample with better field emission characteristics following the LVTF test. Near the sample, Langmuir probe data indicated ion densities on the order of  $10^{15}$   $m^{-3}$ , and Faraday probe data suggested ion energies of  $\sim 20$  eV. Note that the portion of the BN film exposed to the plasma appeared to have been stripped away. However, post-LVTF emission is visible in the exposed region of the film, despite the dramatically different surface morphology.

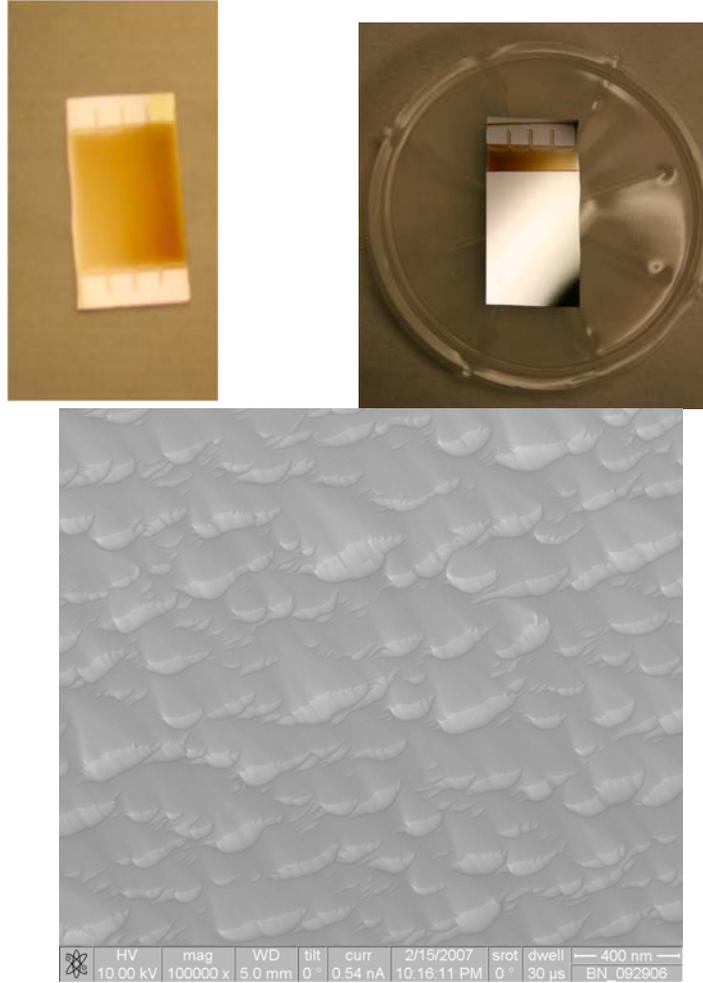
Figure 7 shows the electron emission data for the BN sample under consideration. Although the sample exhibited variance over different voltage sweeps as different emission sites turned on and off, the emission threshold systematically shifted to lower voltages after the BN sample had been placed in the LVTF. As indicated by the linear nature of the Fowler-Nordheim (F-N) plots, electrons are being emitted via a field effect process, which obeys the following relations (with  $c_0$ ,  $c_1$ , and  $c_2$  being constants dependent on the cathode material and configuration):

$$J = \frac{I}{A_e} = A_{FN} E_s^2 \exp\left(-\frac{B_{FN}}{E_s}\right), \quad (1)$$

$$A_{FN} = c_0 \frac{1}{\phi_w} \exp\left(\frac{c_1}{\sqrt{\phi_w}}\right), \quad (2)$$

$$B_{FN} = c_2 \phi_w^{\frac{3}{2}}, \quad (3)$$

$$E_s = \frac{\beta V}{d}. \quad (4)$$



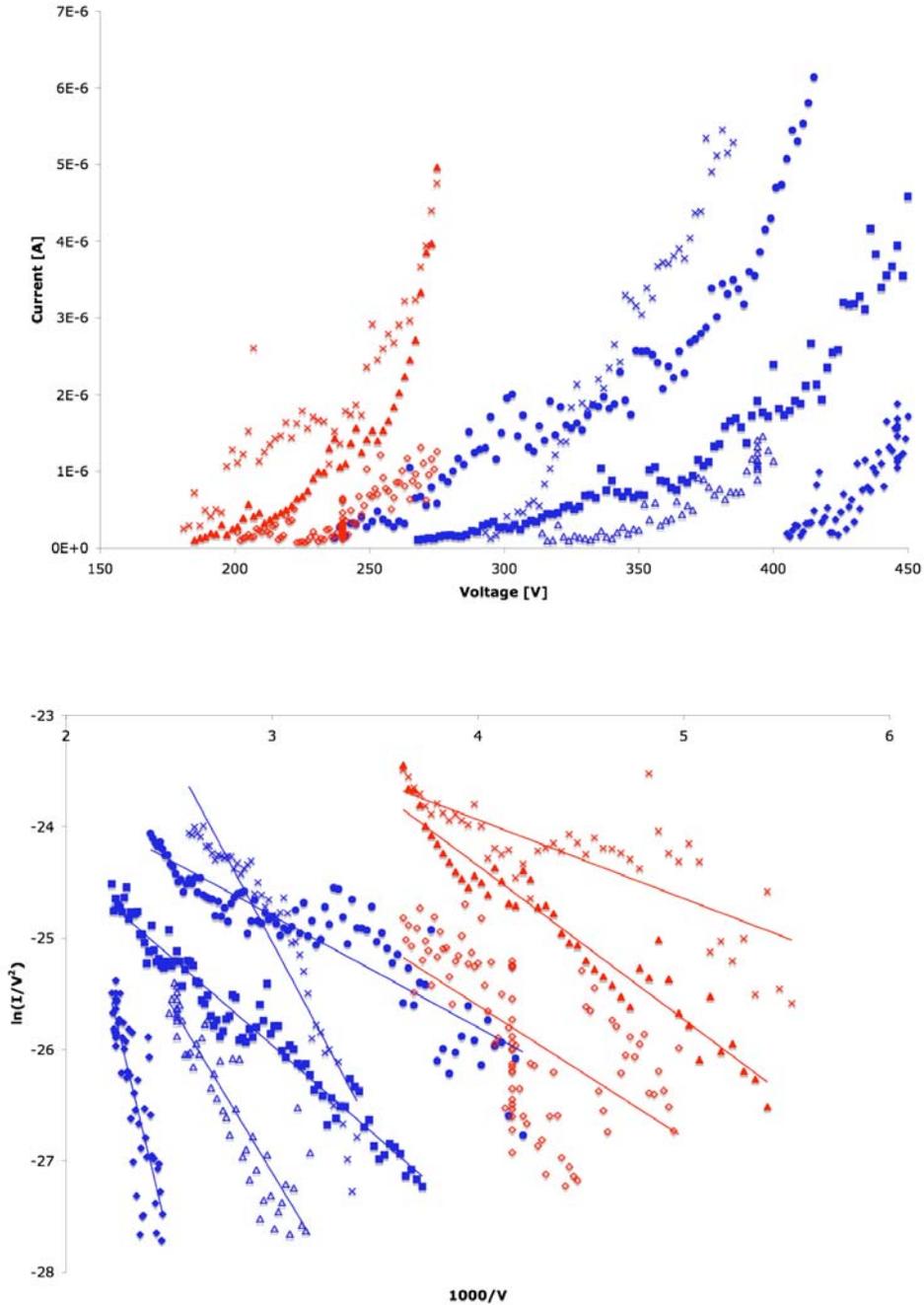
**Figure 6. BN sample that exhibited better field emission characteristics following exposure to Hall thruster environment.** (Upper left) Pre-LVTF. (Upper right) Post-LVTF; lower portion of sample was not covered by tantalum sleeve and exposed to plasma. (Bottom) SEM view of emission region showing different surface morphology than typical BN films.

In a F-N plot of  $V^{-1}$  versus  $\ln(I/V^2)$ , the slope is thus

$$m_{FN} = -c_2 \frac{\phi_w^{\frac{3}{2}} d}{\beta}, \quad (5)$$

and the y-intercept is

$$y_{FN} = \ln \left( c_0 \frac{A_e \beta^2}{\phi_w d^2} \right) + \frac{c_1}{\sqrt{\phi_w}}. \quad (6)$$



**Figure 7. Pre-LVTF and post-LVTF electron emission data.** Each marker symbol (blue for pre-LVTF and red for post-LVTF) represents a single voltage sweep. (Top) Voltage-current measurements. (Bottom) FN transformation of voltage-current data with corresponding linear fits.

In the F-N plot in Figure 7, the slopes are comparable, but the y-intercepts for the post-LVTF data set are generally larger than those for the pre-LVTF data set. This trend suggests, if BN is assumed to be the emission material in both cases, that both the field enhancement factor and the work function may have decreased following

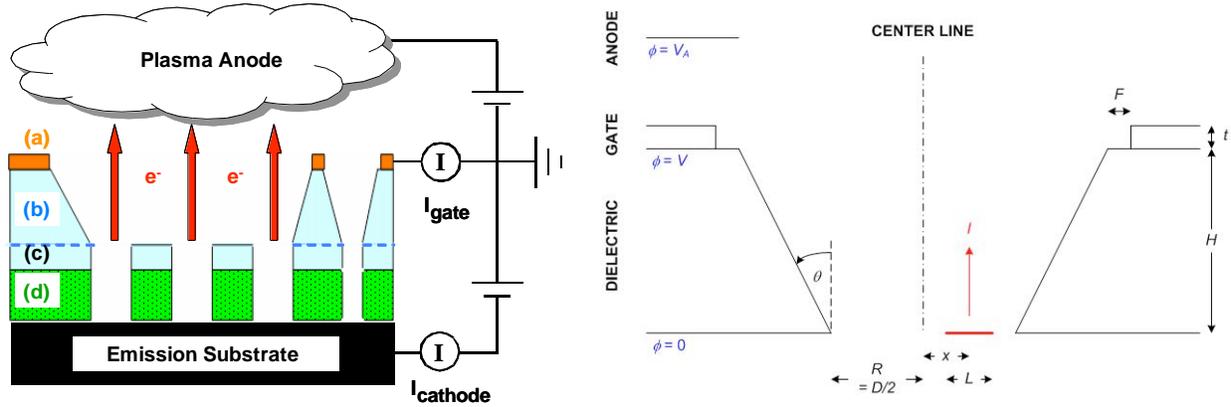
plasma exposure; emission may then be due to residual c-BN clusters on the textured substrate surface. Additional testing and diagnostics (e.g., x-ray photoelectron spectroscopy) are required to verify if alternative causes (e.g., emission due to the textured silicon itself or contaminants deposited by thruster firing) may explain the behavior. Other samples from the LVTF test showed similar results, though additional testing is required to acquire a sufficient statistical average across samples to verify the effect. To address the apparent film degradation, observations of thicker BN films ( $> 100$  nm thickness) in a similar plasma environment are being planned.

### III. MEMS Gates

To form functional FECs, microelectromechanical (MEMS) gate electrodes were developed to extract and accelerate electrons from the BN emission substrates. These MEMS gates are attractive for field emission applications because they are able to achieve micron-scale or smaller gap distances, thus permitting generation of large electric fields at modest bias voltages. MEMS gates can also be used to form scalable arrays to satisfy current requirements while providing size and shape flexibility. Finally, the use of existing microfabrication techniques that are routinely used in the semiconductor and MEMS industries, along with the economies of scale associated with mass production, make MEMS gates potentially economically attractive.

#### A. Gate Design

Figure 8 shows a cross-section schematic of a FEC using a field emission substrate integrated with a MEMS gate. Each MEMS gate consists of a conductive layer placed over a dielectric spacer with channels arrayed throughout the structure to permit passage of electrons. A voltage bias applied between the conductive layer and the emission substrate generates the electric fields needed to extract and accelerate electrons. The thinner the dielectric spacer is, the lower the bias voltage needed to generate the necessary electric fields; the limit is imposed by the breakdown strength of the dielectric material and the structural integrity of the overall gate. Both the conductive and dielectric gate layers are structurally supported in bulk silicon, and viewing windows are periodically etched in the bulk silicon to expose the emission channels.

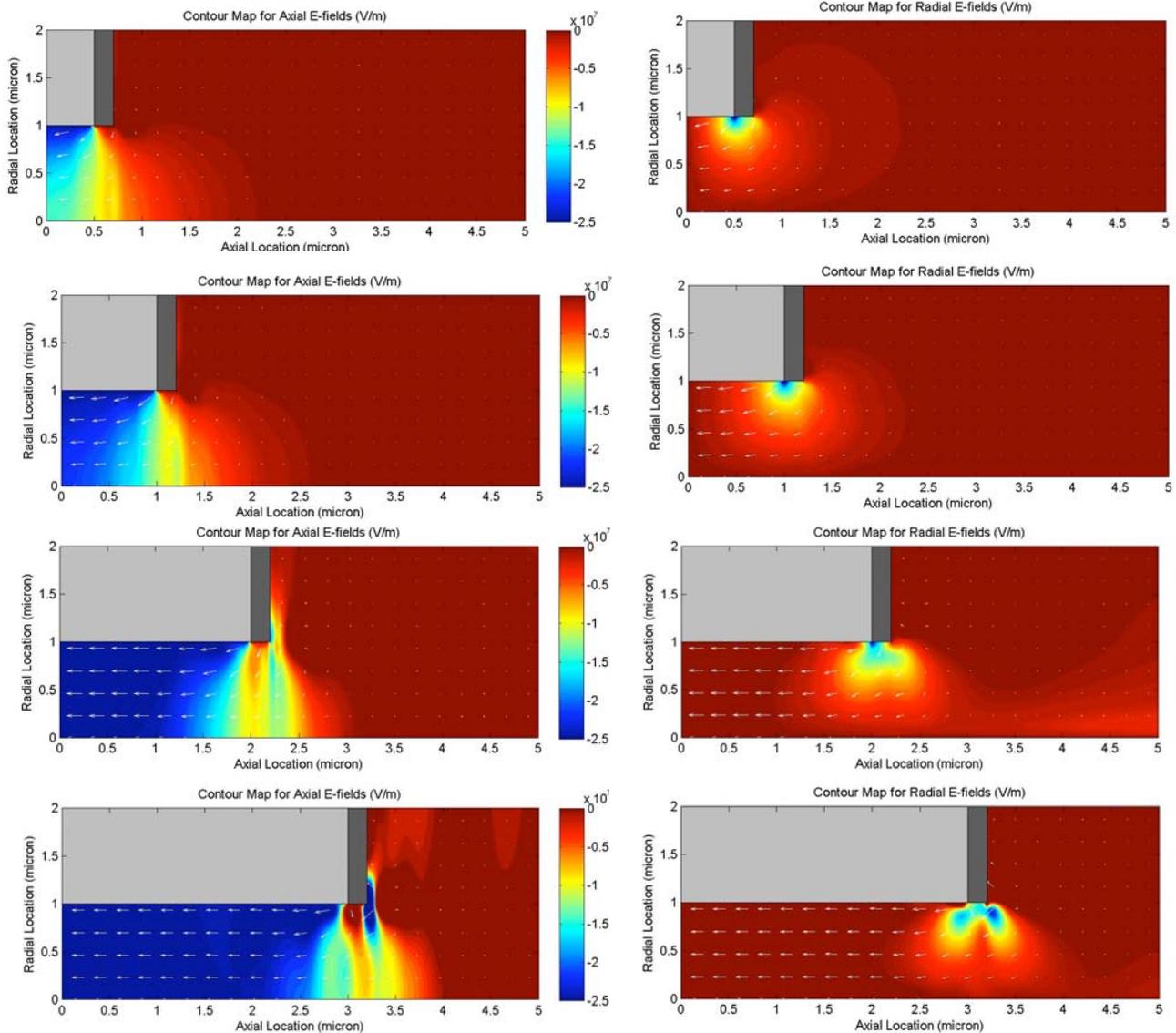


**Figure 8. Proposed use of MEMS gates on FECs.** (Left) Cross-section (not to scale) of MEMS-gated FEC emitting into ambient plasma with (a) electrical contact pad to gate, (b) bulk silicon structural layer, (c) sub-micron conductive gate layer, and (d) dielectric spacer. (Right) Geometric design variables for single emission channel in MEMS gate.

As electrons are emitted through the channels, some electrons impact either the conductive layer or the dielectric spacer due to non-uniformities in the electric field or emission substrate as well as space charge spreading of the electron beam. This collected gate current is an efficiency loss for the system, so a good gate design seeks to minimize gate current. A way to optimize the gate design is to adjust the aspect ratio of the emission channel height to its diameter,

$$A \equiv \frac{H}{D} = \frac{H}{2R}. \quad (7)$$

Previous particle-in-cell simulations have suggested that when all other geometric design variables are fixed and both the emission current and the nominal gap electric field  $V/H$  are constant, the gate current is minimized when the aspect ratio is in the approximate range between 1 and 1.5 (Reference 6). At very high aspect ratios, gate current is higher because of beam spreading before the beam passes the gate. At low aspect ratios, the electric field at the emission surface is not uniform and has a significant radial component that spreads the beam and thus contributes to a higher gate current. This behavior can be seen in Figure 9, which contains electric field maps for single emission channels at various aspect ratios. The channel diameter is fixed at  $2\ \mu\text{m}$  while the channel height is adjusted.

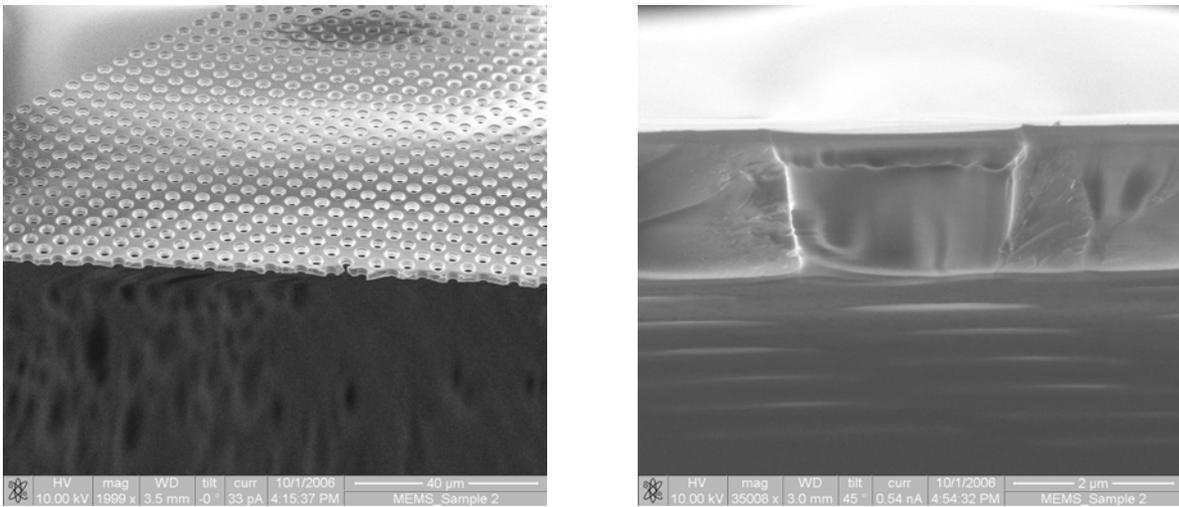


**Figure 9. Electric field maps for various emission channel aspect ratios.** Maps are axisymmetric about the channel centerline  $r = 0$ , and the vectors are for the total electric field. In the simulation domain, the left side boundary (emission surface) is grounded while the right side boundary is kept at the same potential as the gate electrode. This potential bias is scaled linearly with the channel height to maintain a  $25\ \text{V}/\mu\text{m}$  nominal gap electric field. The upper boundary is an insulator at free space permittivity.

Uniform fields at the emission substrate's surface are achieved above a unity aspect ratio. Above an aspect ratio of 1.5, beam-spreading effects begin to dominate while the beneficial effect of additional field uniformity in the emission channel becomes negligible.

## B. Gate Fabrication

The MEMS gates' fabrication process has been previously described (Reference 6). Doped (1-20  $\Omega$ -cm) silicon wafers are used, with one side of the wafer subjected to ion implantation ( $4 \times 10^{16}$ - $\text{cm}^{-2}$  boron at  $\sim 0.5$ - $\mu\text{m}$ -thick) to create the conductive gate electrode. Low-stress silicon oxide nitride ( $\sim 2$ - $\mu\text{m}$ -thick) acts as the dielectric layer, and emission channels are formed via reactive ion etch. A final wet etch opens up emission windows in the bulk silicon to expose the emission channels. Figure 10 shows SEM images of fabricated gates. When nominally designed for a unity aspect ratio using channel diameters of  $\sim 2$   $\mu\text{m}$ , which is near the limit of optical lithography, these gates resulted in reduced aspect ratios between 0.5 to 0.7 as a result of the final wet etch process. Future processing runs, if wet etches are still used, should be able to compensate by nominally designing for a greater than unity aspect ratio; to permit proper growth of the correspondingly thicker dielectric film, stacked film (i.e., alternating layers of silicon oxide and nitride) approaches would be pursued. While current gate designs are stand-alone configurations that must be mounted and integrated with emission substrates, efforts are underway to directly deposit gate layers on BN films to create fully integrated cathode designs. The chief challenges are ensuring proper gate layer adhesion to the BN film and adequate etch selectivity to create the emission channels without damaging the underlying emission substrate.



**Figure 10.** SEM images of MEMS gate. (Left) Isometric view of viewing window with many emission channels. (Right) Cross-section view of an emission channel with less than unity aspect ratio.

## IV. Conclusion and Future Work

While BN films have been successfully grown and tested for electron emission in vacuum and following exposure to a hall thruster environment, more work is needed to improve the film uniformity and to better understand how the film reacts to ambient plasma. Forming regular BN nanotips rather than simply relying on BN films' inherent nanostructure is a potential approach to reduce the threshold electric field for emission, increase the current density, and promote more consistent emission performance. Modeling, fabrication, and testing lessons learned are being applied and extended to other applications, such as the Nanoparticle Field Extraction Thruster (nanofET)<sup>8</sup> requiring MEMS gates.

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